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HI3531DRBCV200

Hisilicon

H.264 Codec processor User Guide

Any questions, please feel free to contact us.
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Hi3531A H.264 CODEC Processor Brief Data Sheet

Key Specifications

Processor Core

- Dual-core ARM Cortex A9@1.1 GHz
 - 32 KB L1 I-cache, 32 KB L1 D-cache
 - 256 KB L2 cache
 - NEON and FPU

Video Encoding/Decoding Protocols

- H.264 baseline/main/high profile L4.2
- MJPEG/JPEG baseline

Video Encoding/Decoding

- H.264&JPEG multi-stream encoding and decoding
 - 8x1080p@30 fps H.264 encoding+8xCIF@30 fps H.264 encoding+4x1080p@30 fps H.264 decoding+8x1080p@2 fps JPEG encoding
 - 16x720p@30 fps H.264 encoding+16xCIF@30 fps H.264 encoding+8x720p@30 fps H.264 decoding+16x720p@2 fps JPEG encoding
 - 32x960H@30 fps H.264 encoding+32xCIF@30 fps H.264 encoding+8x960H@30 fps H.264 decoding+32x960H@2 fps JPEG encoding
 - 32xD1@30 fps H.264 encoding+32xCIF@30 fps H.264 encoding+16xD1@30 fps H.264 decoding+32xD1@2 fps JPEG encoding
- CBR or VBR, ranging from 16 kbit/s to 40 Mbit/s
- Fixed QP
- Encoding frame rate ranging from 1/16 fps to full frame rate
- ROI encoding
- Color-to-gray encoding

Intelligent Video Analysis

- Integrated IVE, supporting various intelligent analysis applications such as motion detection, perimeter defense, and video diagnosis

Video and Graphics Processing

- Video pre- and post-processing, including deinterlacing, sharpening, 3D denoising, DCI, and demosaic
- Anti-flicker for output videos and graphics
- 1/15x to 16x video scaling
- 1/2x to 2x graphics scaling
- Four Cover regions
- OSD overlaying of eight regions

Audio Encoding/Decoding

- ADPCM, G.711, and G.726 hardware audio encoding
- Software audio encoding and decoding complying with multiple protocols

Security Engine

- AES, DES, and 3DES algorithms implemented by using hardware

Video Interfaces

- VI interfaces
 - Eight 8-bit interfaces and one 16-bit video cascade

interface

- Two 8-bit interfaces that can form a 16-bit interface
 - 108 MHz/144 MHz 4xD1/960H TDM inputs for each 8-bit interface (32xD1/32x960H real-time video inputs in total)
 - 144 MHz/148.5 MHz 2x720p TDM inputs for each 8-bit interface (16x720p@30 fps real-time video inputs in total)
 - 4x720p TDM inputs through 148.5 MHz dual-edge sampling or 297 MHz single-edge sampling for each 8-bit interface (32x720p@30 fps real-time video inputs in total)
 - 148.5 MHz BT.1120 inputs in Y/C interleaved mode for each 8-bit interface (8x1080p@30 fps real-time video inputs in total)
 - 2x1080p TDM inputs through 148.5 MHz dual-edge sampling or 297 MHz single-edge sampling for each 8-bit interface (16x1080p@30 fps real-time video inputs in total)
 - 148.5 MHz BT.1120 standard mode for the 16-bit interface (4x1080p@60 fps real-time video inputs in total)
 - One 3840 x 2160@30 fps input through 148.5 MHz dual-edge sampling or 297 MHz single-edge sampling for the 16-bit video cascade input interface
- VO interfaces
 - One HDMI 1.4 output interface with the maximum output of 3840 x 2160@30 fps
 - One VGA HD output interface with the maximum output of 2560 x 1600@60 fps
 - One BT.1120 HD output interface with the maximum output of 1080p@60 fps
 - One BT.1120 cascade output interface with the maximum output of 1080p@60 fps
 - Two independent HD output channels (DHD0 and DHD1), output over any HD interface (HDMI, VGA, or BT.1120/ Cascade Interface)
 - 64-picture output for DHD0, maximum output of 3840 x 2160@30 fps
 - 64-picture output for DHD1, maximum output of 1080p@60 fps
 - One CVBS SD output interface
 - Three full-screen GUI graphics layers in ARGB1555 or ARGB8888 format for two HD channels and one SD channel
 - Two hardware cursor layers in ARGB1555 or ARGB8888 format (configurable) with the maximum resolution of 256 x 256

Audio Interfaces

- Five unidirectional I²S/PCM interfaces
 - Three input interfaces, supporting 20 multiplexed inputs
 - Two output interfaces, supporting the dual-channel output
- 16-bit audio inputs and outputs



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Ethernet Ports

- One gigabit Ethernet port
 - RGMII, RMII, and MII modes
 - 10/100 Mbit/s half-duplex or full-duplex
 - 1000 Mbit/s full-duplex
 - TSO for reducing the CPU usage

Peripheral Interfaces

- Four SATA 3.0/PCIe 2.0/USB 3.0 multiplexed interfaces
 - Configurable four SATA interfaces, two 2-lane PCIe interfaces, two SATA interfaces+two 1-lane PCIe interfaces, or one USB 3.0 interface+two SATA interfaces+one 1-lane PCIe interface
 - RC and EP supported as the PCIe 2.0 interface
 - eSATA and PM supported as the SATA 3.0 interface
 - USB host and hub supported as the USB 3.0 interface
- Two USB 2.0 host interfaces, supporting the hub
- Four UART interfaces (including two 4-wire interfaces)
- One SPI, supporting four CSs
- One IR interface
- Two I²C interface
- Multiple GPIO interfaces

Memory Interfaces

- Two 32-bit DDR3/DDR3L SDRAM interfaces
 - Maximum frequency of 866 MHz
 - Dual channels
 - ODT
 - Maximum capacity of 3 GB
- NAND flash interface
 - 8-bit NAND flash
 - Two CSs
 - SLC or MLC
 - 8-/24-/40-/64-bit ECC (based on 1 KB data block)
- SPI NOR/NAND flash interface
 - 1-/2-/4-bit SPI NOR/NAND flash
 - Two CSs, connected to different types of flash memories
 - Maximum capacity of 32 MB for each CS (only for the

NOR flash)

- Maximum capacity of 4 Gbits for each CS (only for the SPI NAND flash)
- 2 KB/4 KB page size (only for the SPI NAND flash)
- 8-bit/1 KB or 24-bit/1 KB ECC (only for the SPI NAND flash)

- Embedded 4 KB BOOTROM and 64 KB SRAM

RTC with an Independent Power Supply

- Independent battery for supplying power to the RTC

Configurable Boot Modes

- Booting from the BOOTROM
- Booting from the SPI NOR flash
- Booting from the SPI NAND flash
- Booting from the NAND flash
- Booting the slave chip over the PCIe interface

SDK

- Linux 3.10-based SDK
- Audio encoding and decoding libraries complying with multiple protocols
 - High-performance H.264 PC decoding library

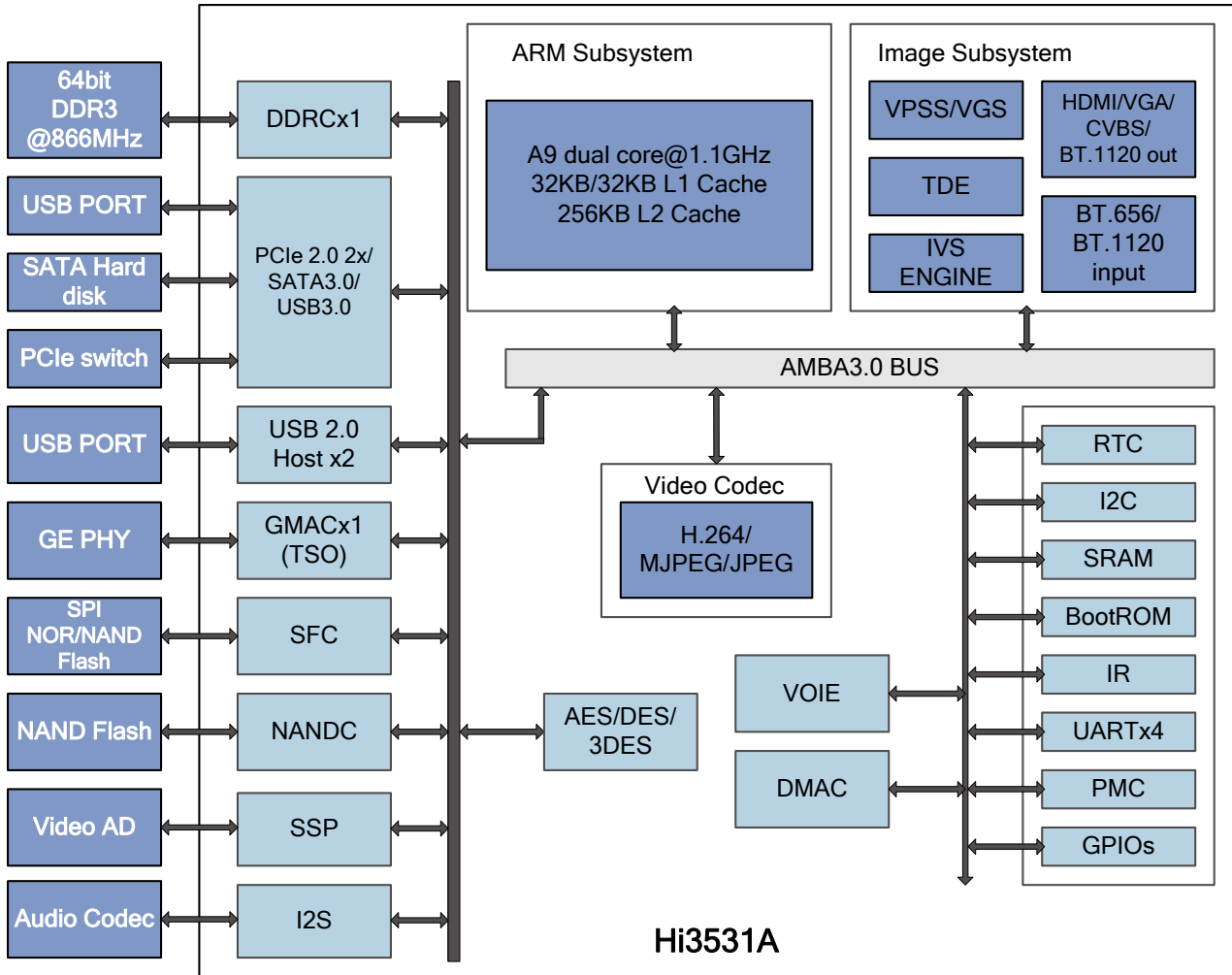
Physical Specifications

- Power consumption
 - Typical power consumption of 5 W
 - Multi-level power consumption control
- Operating voltages
 - 1.1 V core voltage
 - 1.2 V CPU voltage
 - 3.3 V I/O voltage
 - 1.5 V DDR3 SDRAM interface voltage
- Package
 - RoHS, EDHS-PBGA
 - Ball pitch of 0.8 mm (0.03 in.)
 - Body size of 27 mm x 27 mm (1.06 in. x 1.06 in.)
- Operating temperature ranging from 0°C (32°F) to 70°C (158°F)



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Functional Block Diagram



The Hi3531A is a professional SoC targeted for multi-channel HD (1080p/720p) or SD (D1/960H) DVRs. The Hi3531A provides an embedded dual-core ARM A9 processor, a high-performance H.264 video encoding/decoding engine, a high-performance video/graphics processing engine integrated with various complicated graphics processing algorithms, HDMI/VGA HD outputs, and various peripheral interfaces. These features enable the Hi3531A to provide high-performance, high-picture-quality, and low-cost analog HD/SDI solutions for customers' products while greatly reducing the eBOM cost.

DVRs (Each with a Hi3531A)

8x1080p DVR

- 8x1080p@30 fps H.264 encoding+8xCIF@30 fps H.264 encoding+4x1080p@30 fps H.264 decoding+8x1080p@2 fps JPEG encoding
- HDMI 4K x 2K@30 fps output

16x720p DVR

- 16x720p@30 fps H.264 encoding+16xCIF@30 fps H.264 encoding+8x720p@30 fps H.264 decoding+16x720p@2 fps JPEG encoding



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- HDMI 4K x 2K@30 fps output

32x960H DVR

- 32x960H@30 fps H.264 encoding+32xCIF@30 fps H.264 encoding+8x960H@30 fps H.264 decoding+32x960H@2 fps JPEG encoding
- HDMI 4K x 2K@30 fps output+CVBS output

32xD1 DVR

- 32xD1@30 fps H.264 encoding+32xCIF@30 fps H.264 encoding+16xD1@30 fps H.264 decoding+32xD1@2 fps JPEG encoding
- HDMI 4K x 2K@30 fps output+CVBS output

