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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR

2SK3455B

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3455B is N-channel MOS FET device that features a low gate charge and excellent switching characteristics, and designed for high voltage applications such as switching power supply, AC adapter.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3455B-S17-AY Note	Isolated TO-220

Note Pb-free (This product does not contain Pb in External electrode.)

FEATURES

Low gate charge

 $Q_G = 30 \text{ nC TYP}$. (VDD = 400 V, VGS = 10 V, ID = 12 A)

- \bullet Gate voltage rating : $\pm 30~V$
- Low on-state resistance

 $R_{DS(on)} = 0.60 \Omega MAX. (V_{GS} = 10 V, I_{D} = 6.0 A)$

- Avalanche capability ratings
- Isolated TO-220 package

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Ves = 0 V)	VDSS	500	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±30	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	±12	Α
Drain Current (Pulse) Note1	D(pulse)	±36	А
Total Power Dissipation $(T_A = 25^{\circ}C)$	P T1	2.0	W
Total Power Dissipation (Tc = 25°C)	P _{T2}	50	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note2	las	12	Α
Single Avalanche Energy Note2	Eas	103	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = 150 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V

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The mark <R> shows major revised points.

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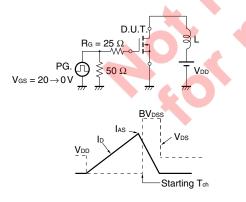
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	loss	Vds = 500 V, Vgs = 0 V			100	μA
Gate Leakage Current	Igss	$V_{GS} = \pm 30 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			±100	nA
Gate Cut-off Voltage	V _{GS(off)}	Vds = 10 V, Id = 1 mA	2.5		3.5	V
Forward Transfer Admittance Note	yfs	Vds = 10 V, Id = 6.0 A	2.0			S
Drain to Source On-state Resistance Note	RDS(on)	Vgs = 10 V, Id = 6.0 A		0.50	0.60	Ω
Input Capacitance	Ciss	Vds = 10 V		1800		pF
Output Capacitance	Coss	V _G s = 0 V		280		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		8		pF
Turn-on Delay Time	td(on)	Vdd = 150 V, Id = 6.0 A		24		ns
Rise Time	tr	V _{GS} = 10 V		14		ns
Turn-off Delay Time	td(off)	R _G = 10 Ω		36		ns
Fall Time	tr			7		ns
Total Gate Charge	QG	Vpd = 400 V		30		nC
Gate to Source Charge	QGS	V _{GS} = 10 V		10		nC
Gate to Drain Charge	Qgd	Ib = 12 A		11		nC
Body Diode Forward Voltage ^{Note}	VF(S-D)	I⊧ = 12 A, V₀s = 0 V		0.9		V
Reverse Recovery Time	trr	IF = 12 A, Vgs = 0 V		440		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/µs		2.6		μC

Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

-ww-c

RG

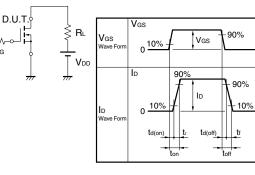
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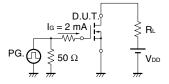
 $\tau = 1 \,\mu s$ Duty Cycle $\leq 1\%$

Vgs

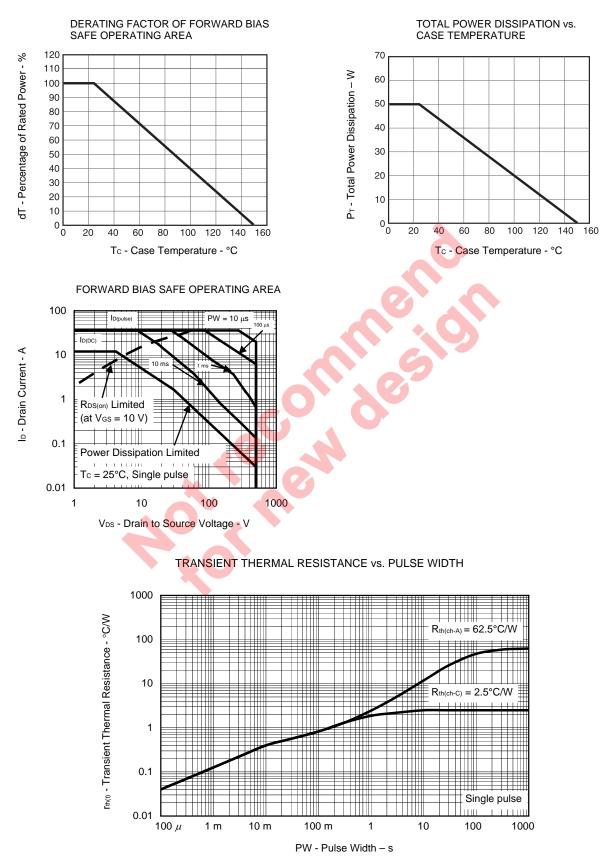
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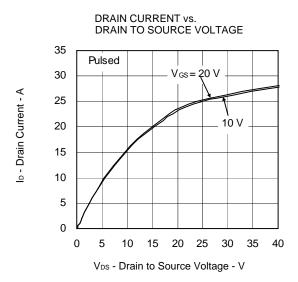
TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS (TA = 25°C)



Data Sheet D18167EJ3V0DS



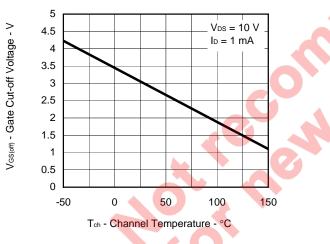
100 $V_{DS} = 10 V$ Pulsed 10 $T_{ch} = -55^{\circ}C$ -25°C 1 25°C 75°C 125°C 0.1 150°C 0.01 10 0 5 15 Vgs - Gate to Source Voltage - V

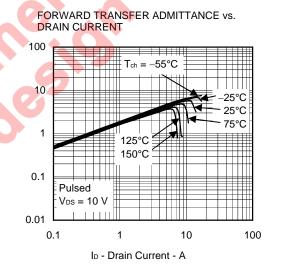
Ip - Drain Current - A

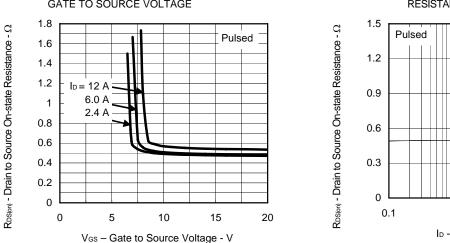
y_{fs} | - Forward Transfer Admittance - S

FORWARD TRANSFER CHARACTERISTICS

GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



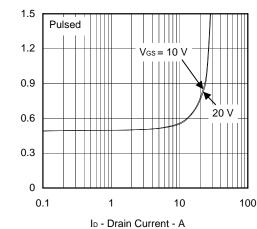




DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

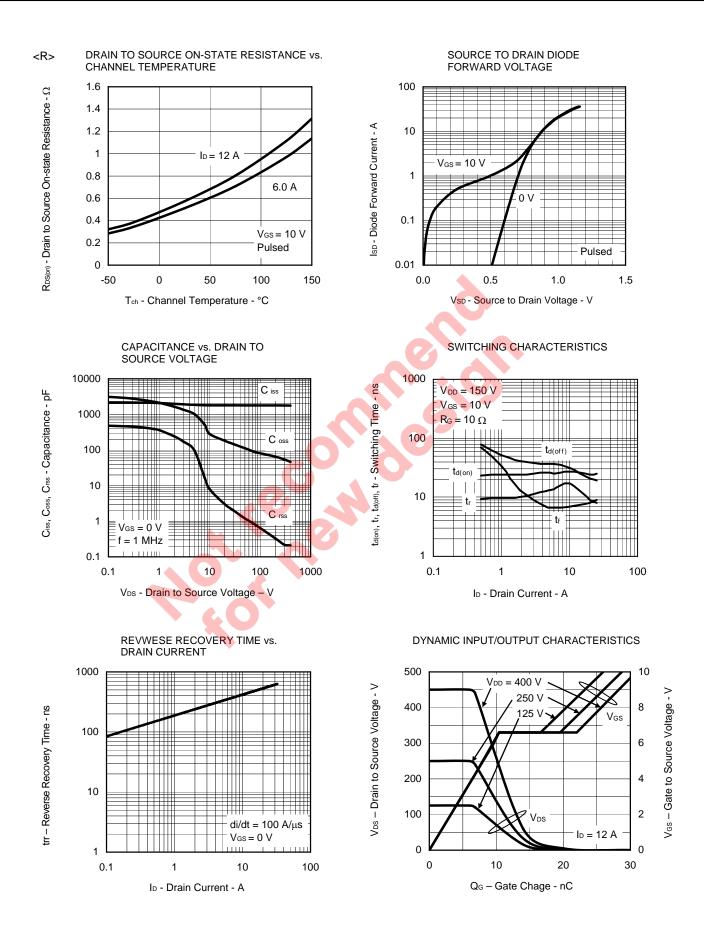
Data Sheet D18167EJ3V0DS

DRAIN TO SOURCE ON-STATE **RESISTANCE vs. DRAIN CURRENT**

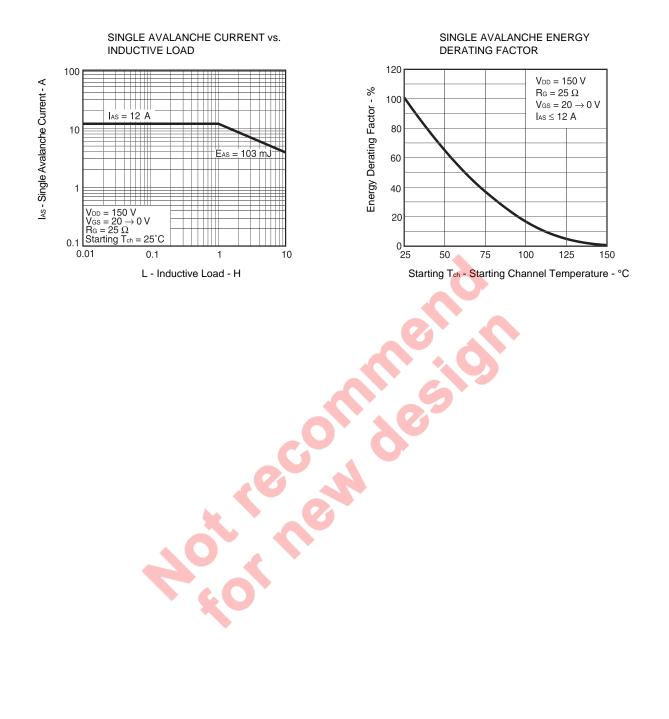


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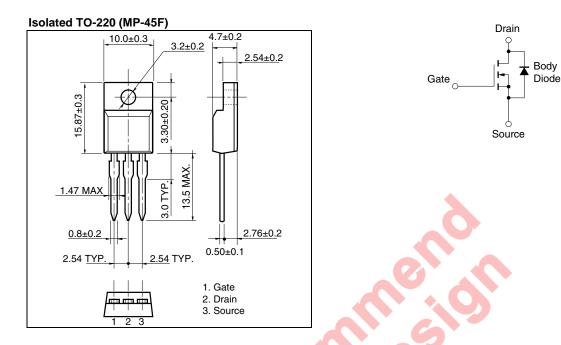


Data Sheet D18167EJ3V0DS



PACKAGE DRAWING (Unit: mm)

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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